AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors, the interface comprising:

an instruction bus, configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU; and

a data bus, coupled to said instruction bus, configured to subsequently transfer the data, wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

2. (currently amended) The interface as recited in claim 1 wherein the plurality of coprocessors comprises:

a first plurality of floating-point coprocessors; or

a first plurality of graphics (3-D) coprocessors~~3-D graphics accelerators~~; or

a second plurality of floating-point coprocessors and a second plurality of graphics (3-D) coprocessors~~3-D graphics accelerators~~.

3. (original) The interface as recited in claim 1, wherein said particular instructions comprise TO instructions, said TO instructions directing that the subsequent transfer of the data will be from the CPU to said designated ones of the plurality of coprocessors.

4. (original) The interface as recited in claim 3, wherein said particular instructions comprise FROM instructions, said FROM instructions directing that the subsequent transfer of the data will be to the CPU from said designated ones of the plurality of coprocessors.

5. (original) The interface as recited in claim 4, wherein said data bus comprises:

data TO signals, for transferring data from the CPU to said designated ones of the plurality of coprocessors; and

data FROM signals, for transferring data to the CPU from said designated ones of the plurality of coprocessors.

6. (original) The interface as recited in claim 5, wherein said data order signals comprise:

TO order signals, for prescribing said data transfer order with respect to transfers via said data TO signals; and

FROM order signals, for prescribing said data transfer order with respect to transfers via said data FROM signals.

7. (original) The interface as recited in claim 6, wherein said TO order signals prescribe a particular outstanding TO instruction relative to all outstanding TO instructions.

8. (original) The interface as recited in claim 6, wherein said FROM order signals prescribe a particular outstanding FROM instruction relative to all outstanding FROM instructions.

9. (currently amended) The interface as recited in ~~claim 1~~claim 1, wherein said data bus transfers the data in parallel to one of said designated ones of the plurality of coprocessors, said one of said designated ones of the plurality of coprocessors having multiple issue pipelines providing for parallel instruction execution.

10. (currently amended) A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a coprocessor interface to be described that transfers data between CPU and a plurality of coprocessors, said computer readable program code comprising:

first program code, for providing an instruction bus, said instruction bus configured to transfer instructions to said plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer said data to/from said CPU; and

second program code, for providing a data bus, said data bus configured to subsequently transfer said data, wherein data order signals within said data bus prescribe a data transfer order that is different from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

11. (original) The computer program product as recited in claim 10, wherein said particular instructions comprise:

TO instructions, said TO instructions directing that the subsequent transfer of said data will be from said CPU to said designated ones of said plurality of coprocessors; and

FROM instructions, said FROM instructions directing that the subsequent transfer of said data will be to said CPU from said designated ones of said plurality of coprocessors.

12. (original) The computer program product as recited in claim 11, wherein said data order signals comprise:

TO order signals, for specifying said data transfer order for a particular outstanding TO instruction relative to all outstanding TO instructions; and

FROM order signals, for specifying said data transfer order for a particular outstanding FROM instruction relative to all outstanding FROM instructions.

13. (currently amended) The computer program product as recited in claim 10, wherein said data bus is configured to transfer said data in parallel to particular coprocessors that have multiple issue pipelines providing for parallel instruction execution and corresponding data transfers.

14. (currently amended) A computer data signal embodied in a transmission medium, the computer data signal comprising:

computer-readable first program code, for providing an instruction bus for transferring instructions to a plurality of coprocessors in an instruction transfer order, wherein particular instructions direct particular coprocessors to transfer data to/from a CPU; and

computer-readable second program code, for providing a data bus for subsequently transferring said data, wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

15. (original) The computer data signal as recited in claim 14, wherein said particular instructions comprise TO instructions, said TO instructions directing that subsequent transfer of said data will be from said CPU to said particular coprocessors.

16. (original) The computer data signal as recited in claim 15, wherein said particular instructions comprise FROM instructions, said FROM instructions directing that the subsequent transfer of said data will be to said CPU from said particular coprocessors.

17. (original) The computer data signal as recited in claim 14, wherein said data bus comprises:

data TO signals, for transferring data from said CPU to said particular coprocessors; and

data FROM signals, for transferring data to said CPU from said particular coprocessors.

18. (original) The computer data signal as recited in claim 17, wherein said data order signals comprise:

TO order signals, for prescribing said data transfer order with respect to transfers via said data TO signals; and

FROM order signals, for prescribing said data transfer order with respect to transfers via said data FROM signals.

19. (original) The computer data signal as recited in claim 18, wherein said TO order signals prescribe a particular outstanding TO instruction relative to all outstanding TO instructions.

20. (original) The computer data signal as recited in claim 18, wherein said FROM order signals prescribe a particular outstanding FROM instruction relative to all outstanding FROM instructions.

21. (currently amended) The computer data signal as recited in ~~claim 1~~claim 14, wherein said data bus transfers said data in parallel to selected coprocessors, said selected coprocessors having multiple issue execution pipelines.

22. (currently amended) A method for transferring data between a CPU and a plurality of coprocessors, the method comprising:

~~a) transmitting~~transmitting instructions to the plurality coprocessors, each of the instructions directing a data transfer between the CPU and a specific coprocessor, wherein said transmitting is provided in a specific instruction order;

~~b) subsequently~~subsequently transferring the data in an order different from the specific instruction order, said transferring comprising:

~~i) prescribing~~prescribing transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions, the outstanding instructions being those instructions that have not completed a subsequent data transfer.

23. (currently amended) The method as recited in claim ~~21~~22, said transmitting comprises:

~~i) issuing~~issuing a plurality of the instructions in parallel to the specific coprocessor; and

~~ii) designating~~designating an execution order corresponding to said issuing.